E/6/1

NEW SCHEME

05EC021

Reg. No. | | | | | | | | | | |

First Semester M.Tech. Degree Examination, January/February 2006

LDS/LEC/LVS/LPE/LIE/LEL

CMOS VLSI Design.

Time: 3 hrs.) (Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) Describe the working on nMOS enhancement mode transistor with diagrams and output characteristics. **(8 Marks)**

   (b) Deduce high frequency small signal equivalent circuit of MOS transistor and an expression for figure of merit. **(6 Marks)**

   (c) What are the advantages of BiCMOS inverter over CMOS counterparts? Draw the circuit diagram of a BiCMOS inverter in which problems associated with static power dissipation and stored charge in the base are eliminated and explain its working. **(6 Marks)**

2. (a) Explain λ based design rules as applicable to MOS layers and transistors. **(8 Marks)**

   (b) Compare CMOS and SOI technology. Draw sketches involved in CMOS inverter fabrication process. **(6 Marks)**

   (c) Define sheet resistance, standard unit of capacitance and delay unit of time. **(6 Marks)**

3. (a) Show that nMOS/CMOS inverter pair delay is invariant. **(6 Marks)**

   (b) A MOS layer is 5λ wide, 60λ long and $1\mu m$ thick. The resistivity of the layer is $1\Omega cm$. Using sheet resistance concept, calculate the resistance of the MOS layer along its length. **(6 Marks)**

   (c) An off chip capacitance load of 20 pF is to be driven by a chain of CMOS inverters of 5μ technology. Compute the number of inverters, width factor and over all delay through the chain for minimum overall delay. Assume C_g for $5\mu m$ technology as 0.01pF and $R_s = 10k\Omega$. **(8 Marks)**

4. (a) Derive an expression for the propagation delay through a chain of pass transistors. **(6 Marks)**

   (b) Draw circuit and stick diagrams of two input NOR gate and 1 bit shift register using CMOS inverters. Standard colour/monochrome codes are to be used for stick diagrams. **(8 Marks)**

   (c) Derive scaling factors of the following MOS parameters using combined voltage and dimension scaling model :

   i) Number of gates - N

   ii) Saturation current - I_{dss}

   iii) Power speed product - P_T **(6 Marks)**

Contd.... 2

5. (a) Distinguish between combinational and sequential circuits. (4 Marks)

(b) Describe the behaviour of two inverter bistable element with one inveter in the feed back loop. Also derive expressions for output voltages of inverters. (10 Marks)

(c) Differentiate between static and dynamic CMOS circuits with relevant diagrams. (6 Marks)

6. (a) Explain how domino circuits evolved from dynamic CMOS circuits and reasons there of. (6 Marks)

(b) Draw nMOS and CMOS version of the circuit to realise the following Boolean expression : (8 Marks)

$z = \overline{A(D+E)+BC}$.

(c) Explain the working of clocked SR latch with the help of circuit diagram and waveforms. (6 Marks)

7. (a) What is latch up in CMOS inverters and how is it minimised? (6 Marks)

(b) Realise NOR and NAND gate functions using transmission gates. (8 Marks)

(c) What are the demerits of n and p pass transistors w.r.t output voltages and how are these overcome in a transmission gate? (6 Marks)

8. Write short notes on :

(a) MOS model

(b) Differential amplifier

(c) Clock generation and distribution

(d) Voltage boot strapping. (4×5=20 Marks)

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NEW SCHEME

M.Tech. Degree Examination, May / June 2006

CMOS VLSI Design

Time: 3 hrs.] [Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain the trends in transfer characteristics with β_n/β_p ratio's, using suitable mathematical analysis. **(10 Marks)**

b. Write an expression for threshold voltage of n - channel E-MOSFET and hence explain the role of each term in the equation. Modify this equation suitably so as to express the same for $V_{SB} = 0$ **(10 Marks)**

2 a. Estimate the ON state resistance of the inverter circuit shown in figure 2(a), using the concepts of sheet resistance. Assume 5 μ m technology. Given the following data, also estimate current between power lines. Derive the formula used for calculations.

LAYER	R_S ohm per square		
	5 μ m	orbit	orbit 1.2 μ m
n-transistor channel	10^4	2×10^4	2×10^4
p-transistor channel	2.5×10^4	4.5×10^4	4.5×10^4

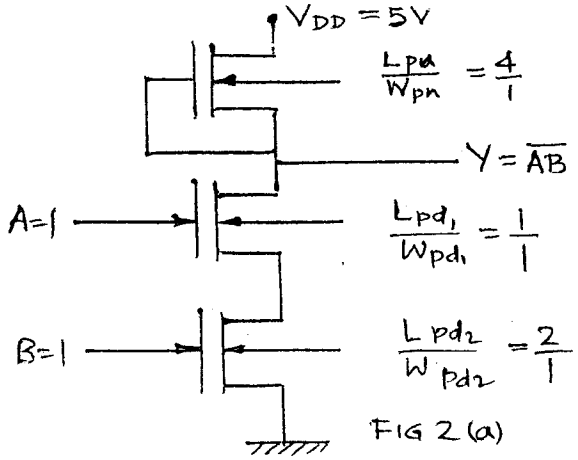

FIG 2(a)

(10 Marks)

b. Explain the significance of channel length modulation and hot electron effect in MOS devices. **(10 Marks)**

3 a. Explain the operation of MOSFET in CS configuration when the load to the devices are i) Resistive load, ii) Diode – connected load, iii) Current source load. **(15 Marks)**

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b. For the circuit shown in figure 3(b), calculate the small signal voltage gain of the circuit.

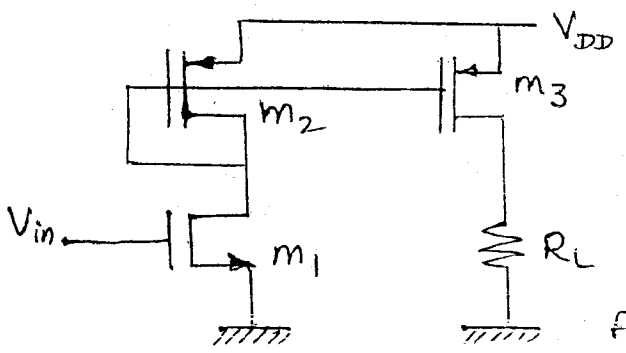

Fig 3(b)

(05 Marks)

4 a. Explain the fabrication process of P well CMOS inverter with neat sketches where ever necessary. (10 Marks)

b. What are lambda based design rules? Bring out the merits and demerits there of. (10 Marks)

5 a. Draw symbol diagram of a two bit CMOS shift registers, reducing the number of transistors wherever possible. (10 Marks)

b. Draw nMOS, CMOS version of the circuit to realise the boolean expression.

$$Z = \overline{(D+E+A)(B+C)}$$

(10 Marks)

6 a. Derive an expression for figure of merit of n channel E-MOSFET. (10 Marks)

b. Explain the working of CMOS transmission sate with its equivalent resistance curve. What are the advantages of transmission gate ? (10 Marks)

7 a. What is domino CMOS logic? Compare it with conventional CMOS logic. Justify the same with one example each. (10 Marks)

b. Explain how clock signal can be generated, distributed and stored in dynamic CMOS inverter circuits. (10 Marks)

8 Write technical note on the following :

a. Bi-CMOS inverter

b. Pass transistor circuit

c. Punch through conditions in MOS transistor.

d. CMOS D latch. (20 Marks)

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05EC021

USN

NEW SCHEME

First Semester M.Tech. Degree Examination, Dec.06/Jan. 07

CMOS VLSI Design

Time: 3 hrs.] [Max. Marks:100

Note: *1. Answer any FIVE full questions.*
2. Assume missing data if any.
3. Draw neat diagrams where ever necessary.
4. Show complete solutions to the derivations/problems step by step.

1 a. Write an expression for threshold voltage of n channel E MOSFET and hence explain the significance of each term in this equation. Also explain the concepts of sub threshold voltage and sub threshold current. **(10 Marks)**

b. Draw a neat circuit of biased n channel E MOSFET operating in inversion mode and hence explain the concept of hot electron effect and punch through conditions, suggest any remedy if any to over come the problem of hot electron effect. **(10 Marks)**

2 a. Explain the transfer plot of CMOS inverter with necessary mathematical analysis for different values of $\beta n / \beta p$ ratios. **(10 Marks)**

b. Calculate the native threshold voltage for a n channel MOSFET at 300K for a process with a silicon substrate with $Na = 1.80 \times 10^{16}$, a SiO_2 gate oxide with thickness 200Å. Assume $\Phi_{ms} = -0.9$ volts, $Q_{fe} = 0$. **(10 Marks)**

3 a. With suitable mathematical analysis explain the transfer plot of MOS inverter with static load and pseudo n MOS inverter for different values of aspect ratios. **(10 Marks)**

b. Explain in detail the double metal MOS process rules for a VLSI technology. **(10 Marks)**

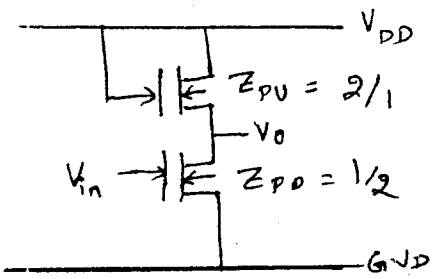
4 a. Describe in detail twin well CMOS process of fabrication. **(10 Marks)**

b. Calculate the time for free electrons to cross a n – channel E – MOSFET of channel length 3 microns. If Vdd = 5V, assume saturation velocity of electrons, $= V_n = 5 \times 10^7$ cm/sec and mobility of electrons = 800 $cm^2 / V - sec$. **(10 Marks)**

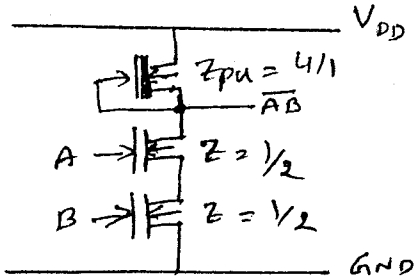
5 a. Show that as the RC delay lines approach infinity, the signal delay reduces when inverters are connected in cascade. **(10 Marks)**

b. Draw stick diagram for the following : **(10 Marks)**

(i)



(ii)



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6 a. With neat diagrams explain the construction and working principles of voltage bootstrapping synchronous dynamic circuit. (10 Marks)

b. Describe the construction and working principles of MOS differential amplifier driven by a constant current source and hence derive an expression for voltage gain of the amplifier. (10 Marks)

7 a. Describe with neat figures the fabrication of N WELL CMOS. (10 Marks)

b. Explain the operation of CMOS SR Latch and clocked JK Latch (10 Marks)

8 Write technical notes on the following :

a. SOS technology.

b. Clocked storage elements. (20 Marks)

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E/b/4

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NEW SCHEME

First Semester M.Tech. Degree Examination, June 2007
CMOS VLSI Design

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Starting from the fundamentals, derive an expression for threshold voltage in a MOS transistor. **(06 Marks)**

b. Briefly explain the following terms: i) Channel length modulation ii) Fowler – Nordheim tunneling iii) Impact ionization. **(08 Marks)**

c. With a neat diagram showing the levels of various voltages and transfer characteristic explain the noise margin. **(06 Marks)**

2 a. Explain the working of differential inverter with a neat diagram and the transfer characteristics. **(06 Marks)**

b. With respect to: i) Change in control input ii) Change in switched input, explain the transmission gate output characteristics. **(06 Marks)**

c. Discuss the various circuit arrangements to be employed in BICMOS inverters. **(08 Marks)**

3 a. Explain with neat sketches the lambda bared design rules with respect to wires, transistors and contacts. **(08 Marks)**

b. With a neat structure (final diagram) explain the twin-tub CMOS process. **(06 Marks)**

c. Bring out the differences between metal interconnect and polysilicon / refractory metal interconnect. **(06 Marks)**

4 a. Show that the transit time and time delay are interchangeable in CMOS technology. **(08 Marks)**

b. Derive an expression for total delay when number of stages N is odd and even while driving large capacitive loads. **(08 Marks)**

c. Draw the CMOS circuit diagram and the stick diagram for a 2 input NAND gate. **(04 Marks)**

5 a. With a neat CMOS circuit diagram showing the parasitic capacitance explain 2 input CMOS NOR gate and specify the condition for K_n and K_p to get $V_{th} = V_{DD}/2$. **(07 Marks)**

b. Bring out the differences between AND-OR-inverter (AOI) logic and OR-AND-inverter (O-A-I) logic with a suitable example. **(06 Marks)**

c. Explain briefly the SR latch with gate level schematic truth tables and CMOS circuit. **(07 Marks)**

6 a. Explain the phenomenon of charge storage and charge leakage and obtain the expression for the holding time t_{hold}. **(07 Marks)**

b. Dynamic CMOS logic circuits cannot be cascaded. Why? Explain. **(06 Marks)**

c. Discuss the pipelined NORA CMOS system with relevant diagrams. **(07 Marks)**

7 a. Explain the differential amplifier with a neat CMOS circuit and cross-section. Obtain the expression for transconductance of differential amplifier. **(10 Marks)**

b. Starting from the fundamentals derive an expression for the reference voltage V_{REF} in a conventional CMOS band gap reference. **(10 Marks)**

8 a. Explain the latch up phenomenon in a CMOS structure with the help of cross sectional view, circuit model and V-I characteristics. **(08 Marks)**

b. Bring out the differences between NMOS and CMOS fabrication processes. **(05 Marks)**

c. Explain the various techniques employed for generation of clock in CMOS technology. **(07 Marks)**

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05EC021

M.Tech. Degree Examination, Dec. 07 / Jan. 08
CMOS VLSI Design

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Briefly explain the second order effects in MOSFET. **(07 Marks)**

b. With neat diagram and transfer characteristics, explain the CMOS inverter. Obtain the necessary expressions for the same. **(08 Marks)**

c. Calculate the native threshold voltage for an n-transistor at 300^0 k for a process with a silicon substrate with $N_A = 1.8 \times 10^{16}$ /cc, $t_{ox} = 200\,\text{Å}$. Assume $\phi_{ms} = -0.9V$, $Q_{fc} = 0$, $\eta_I = 1.45 \times 10^{10}$ /cc. **(05 Marks)**

2 a. With relevant response curves, explain the transmission gate output characteristics for change in control input and for change in switched input. **(06 Marks)**

b. Obtain the scaling factors for the following – i) Gate delay ii) Current density iii) Switching energy. **(06 Marks)**

c. With neat fabrication sketches. Explain the silicon on insulator (SOI) COMS process. **(08 Marks)**

3 a. Explain the CMOS process enhancement with reference to i) metal interconnect ii) polysilicon /refractory metal inter connect. **(06 Marks)**

b. For the following structure obtain values for Cm, Cp, Cg and C_T. Given that the relative values of capacitances are metal 1 = 0.075 □ Cg, polysilicon = 0.1 □ Cg.

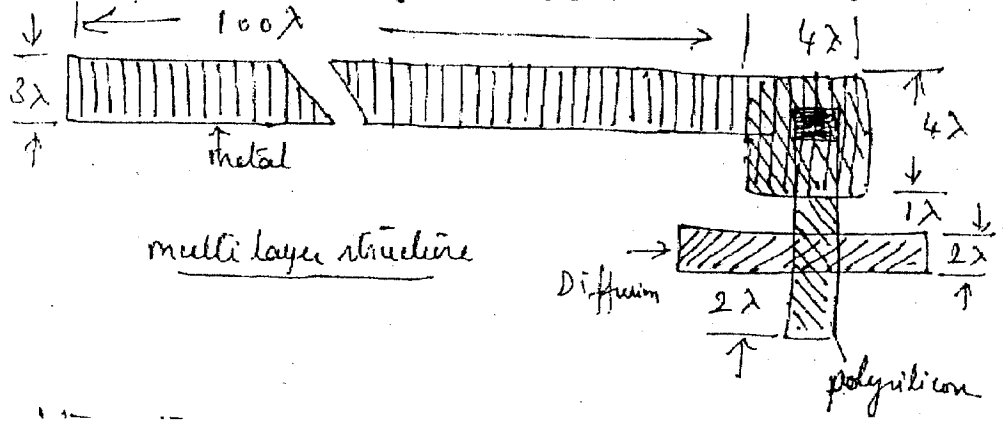

Fig. Q 3(b) **(08 Marks)**

c. Obtain the CMOS circuit and stick diagram for the following function $f = \overline{(A+BC)D}$. **(06 Marks)**

4 a. With a neat diagram, obtain the parasitic device capacitance in CMOS 2 input NOR gate for kN = 4 KP and explain the circuit operation. **(06 Marks)**

b. Differentiate between AOI logic and OAI logic with a suitable example of each. **(08 Marks)**

c. For the given function F = AB + A'C' + AB'C obtain the i) CMOS TG realization
ii) COMS transistor realization. **(06 Marks)**

5 a. With a neat gate level schematic and CMOS circuit explain the CMOS SR latch circuit based on clocked NOR2 gates. (06 Marks)

b. Briefly discuss the charge storage and charge leakage in n mos pass transistor. (06 Marks)

c. Calculate the worst case time for the following data given $V_{TO} = 0.8$ V, $\nu = 0.4\ V^{1/2}$, $|2\phi_F| = 0.6V$, $C_{OX} = 0.065$ f F /μ m^2, $C^1_{metal} = 0.036fF/\mu m^2$, $C^1_{poly} = 0.055fF/\mu m^2$, $C_{jo} = 0.095$ f F/μ m^2, $C_{josw} = 0.2$ f F/μ m. $I_{leakage} = 0.85$ pA.

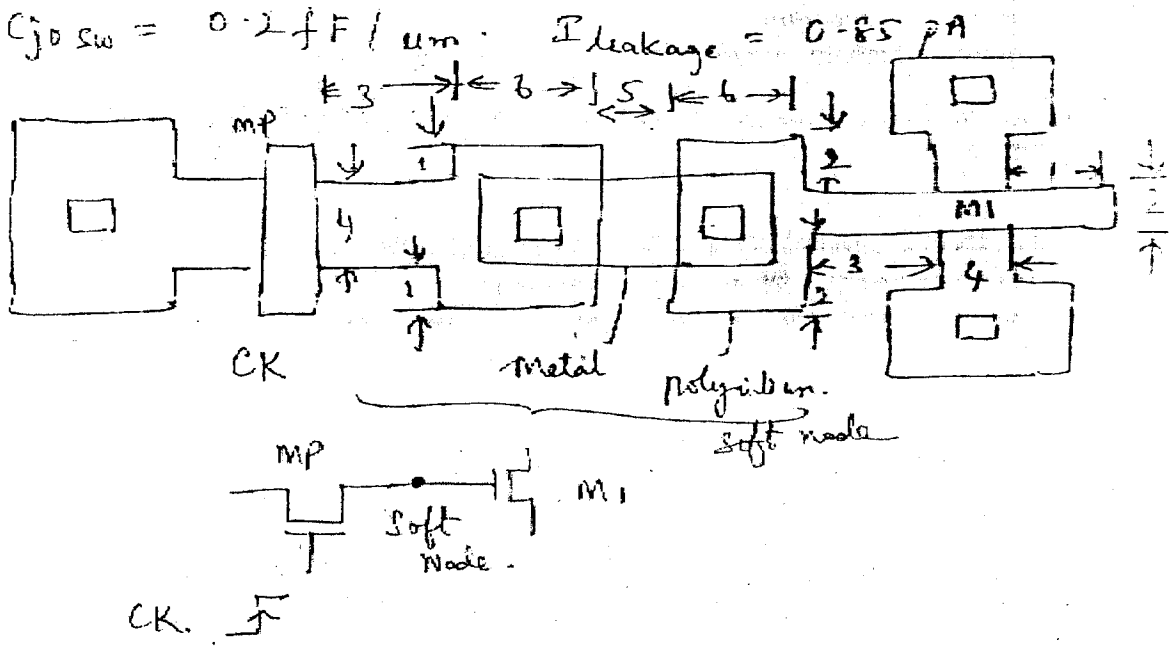

Fig. Q 5(c) (08 Marks)

6 a. Bring out the difference between Ratioed logic and ratio less logic with respect to 3 bit shift register. (06 Marks)

b. Dynamic CMOS logic circuit cannot be cascaded. Justify the statement. (06 Marks)

c. With relevant diagram, explain the NORA CMOS logi e[NP – Domino logid]. (08 Marks)

7 a. Explain with necessary expressions and transfer characteristics the differential amplifier. (08 Marks)

b. Discuss the general principle of the Band-gap reference and hence obtain expression for V_{BE}. (07 Marks)

c. Briefly explain the clock distribution network with relevant sketches. (05 Marks)

8 Write short notes on : (10 Marks)

a. Differential inverter

b. Complementary pass transistor logic (CPL)

c. Domino CMOS logic

d. Latch up phenomenon. (10 Marks)

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08EC021

M.Tech. Degree Examination, Dec.08/Jan.09
CMOS VLSI Design

Time: 3 hrs. Max. Marks:100

Note: 1. ***Answer any FIVE full questions.***
2. ***Assume missing data if any, suitably.***

1 a. How does the nmos-enhancement mode transistor function, in different regions of operation? Explain with neat sketches and output characteristics. (08 Marks)
b. What are the second order effects in a MOSFET? Explain. (12 Marks)

2 a. With neat fabrication sketches, explain the fabrication of a cmos inverter. (12 Marks)
b. Obtain the scaling factors for the following gate capacitance C_g, gate delay T_d, Maximum operating frequency f_0 and current density J. (08 Marks)

3 a. Define sheet resistance, standard unit of capacitance and delay unit J. (06 Marks)
b. Derive the expressions for rise time and fall time of a cmos inverter. (08 Marks)
c. A mos layer in 5 μm wide, 60 μm long and 1 μm thick. The resistivity of the layer is 1 Ωcm. Using the sheet resistance concept, calculate the resistance of the mos layer along its length. (06 Marks)

4 a. Provide the λ-based design rules for double metal, cmos process technology, for all layers, transistors and contacts. (10 Marks)
b. Draw the cmos circuit and stick diagram for the function $\overline{(AB+C)D}$. (06 Marks)
c. What are the disadvantages of nmos and pmos pass transistors? How is the transmission gate useful in this regard? (04 Marks)

5 a. With a neat circuit diagram, showing the parasitic capcitance, explain cmos 2 input NOR gate and specify the condition for Kn and Kp to get $Vth = \frac{VDD}{2}$. (08 Marks)
b. Realize the functions,
i) $A = xy + x'y' + xy'z$ and
ii) $B = x'y + xy'$
using transmission gates. (06 Marks)
c. Draw the cmos logic circuit for the function $\overline{(D+E+A)(B+C)} = Z$. (06 Marks)

6 a. Explain the function of a SR latch using NAND2 gates with gate level schematic and cmos circuit. (06 Marks)
b. What is voltage boot strapping? Explain. (08 Marks)
c. Explain the phenomenon of charge storage and charge leakage in a nmos pass transistor. (06 Marks)

7 a. Explain the operation of a cmos differential amplifier with neat circuit. (08 Marks)
b. Describe the different clock distribution schemes. (06 Marks)
c. With neat circuit diagram explain NORA CMOS logic (NP – Domino logic). (06 Marks)

8 Write short notes on:
a. Domino cmos logic.
b. Bicmos circuits.
c. Cmos process enhancement.
d. S.O.I technology. (20 Marks)

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M.Tech. Degree Examination, Dec.09/Jan.10

CMOS VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. With neat sketches, explain the behaviour of nMOS device under the influence of different terminal voltages (Enhancement mode). **(09 Marks)**

b. Explain small signal model for an MOS transistor. **(06 Marks)**

c. Write a note on differential inverter. **(05 Marks)**

2 a. Explain λ based design rules. **(08 Marks)**

b. Obtain the scaling factors for the following:

i) Gate capacitance C_g

ii) Saturation current I_{dss}

iii) Parasitic capacitance. **(06 Marks)**

c. Define sheet resistance and also explain the concept applied to MOS transistor and inverters. **(06 Marks)**

3 a. Explain the second order effects associated with a MOSFET. **(10 Marks)**

b. Explain twin tub CMOS process. **(10 Marks)**

4 a. Explain the effect of long polysilicon wires. Show how to improve the signal propagation. **(04 Marks)**

b. Derive the threshold voltage equation (V_t) for 2 inputs CMOS NOR gate ($V_{t\,NOR2}$). **(10 Marks)**

c. For the given function $f = \overline{A}B + A\overline{C} + A(B + D)$, obtain

i) CMOS TG realization

ii) CMOS transistor realisation **(06 Marks)**

5 a. Explain the function of D latch with gate level schematic and CMOS circuit. **(06 Marks)**

b. Explain synchronous dynamic circuit implemented using depletion load nMOS. **(09 Marks)**

c. Explain the principle of pass transistor circuit. **(05 Marks)**

6 a. Discuss the general principle of band gap reference and hence obtain expression for V_{BE}. **(08 Marks)**

b. Explain cross operational amplifier with necessary expression and characteristics. **(08 Marks)**

c. Mention the advantages of CMOS over NMOS. **(04 Marks)**

7 a. Describe different clock distribution schemes. **(06 Marks)**

b. Mention the causes of latch up and guidelines for avoiding latch up. **(10 Marks)**

c. Realize the following function Z = AB + (C + D) (E + F) + GH using

i) Standard CMOS

ii) Domino CMOS. **(04 Marks)**

8 Write short notes on:

a. BICMOS circuit

b. Dynamic CMOS logic

c. Voltage boot strapping

d. Current mirror. **(20 Marks)**

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